REMARKS

Applicants respectfully request reconsideration and allowance of the subject application. Claims 1, 3-9, 12, 16-21, 23, 26, 26 and 29-47 are pending in the application.

Allowable Claims

Claims 29-32 would be allowable if a terminal disclaimer were filed to overcome the double patenting rejection. Applicants thank the Examiner for this indication of allowable subject matter. Claims 29-32 remain unchanged and pending in the application. Applicants request that the rejection of Claims 29-32 be held in abeyance pending further examination of the other claims pending in the application.

Claim Rejection under 35 U.S.C. § 102

Claims 1-7 and 9-27 stand rejected under 35 U.S.C. § 102 as being anticipated by "Power Aware Page Allocation" by Lebeck et al. Applicants traverse.

The Lebeck Reference

Lebeck describes an "abstract model" of storing code and data in multiple independently controlled memory chips each having multiple power states. Lebeck discloses that pages of code and data may be stored according to a random placement policy or a sequential placement policy (e.g., sequential first-touch). According to the random placement policy, the operating system randomly chooses a memory chip for storing each page in a memory instruction. According

to the sequential placement policy, the operating system sequentially stores the pages of a memory instruction in a given memory chip until the entire chip is filled before moving on to the next chip. Both random and sequential placement policies are performed at the time that the content is first saved in the physical memory. Lebeck teaches that if a sequential placement policy is utilized, the contents in the physical memory may be reorganized one time to cluster the most frequently accessed pages in a particular memory chip (e.g., frequency placement policy). Finally, Lebeck discloses that each (e.g., dynamic power management policy) or all (e.g., static power management policy) of the memory devices are set to a reduced power mode after a static threshold period of time from the last memory access.

Claim 1

Claim 1, as amended, recites "creating mappings from received addresses to physical memory by a hardware interface disposed between a processor and a number of physical memory devices" and "modifying the mappings by the hardware interface . . .." Lebeck does not teach or suggest that mappings are created or modified at a hardware interface disposed between a processor and the physical memory devices. Instead, Lebeck discloses that a reassignment is performed by the operating system. Specifically, Lebeck teaches "the OS sorts the counters and performs the movement and repacking operations, and resumes program operation," section 6.3. Since the OS is executed by the processor, it is clear that Lebeck's processor itself performs reassignment.

Thus, Lebeck does not disclose that the mappings are created and modified at a hardware interface disposed between a processor and the physical memory

devices. Therefore Applicants respectfully submit that Claim 1 is patentable over Lebeck. Applicants respectfully request that the §102(a) rejection of Claim 1 be withdrawn and Claim 1 be allowed.

Claims 2 and 39-47

Dependent Claims 39-47 are allowable by virtue of their dependency on respective base Claim 1, as well as the additional elements they recite. With respect to Claim 39, the additional elements include "receiving memory instructions from a processor or graphics adapter by the hardware interface." Lebeck does not teach or suggest that the memory instruction are received by a hardware interface that is disposed between the processor and the memory. Accordingly, those skilled in the art would appreciate that the systems and methods of Lebeck would not permit memory access by other sources such as a graphics adapter. Accordingly, Applicants respectfully submit that Claim 39 contains elements that are not disclosed by Lebeck and therefore is patentable over Lebeck.

With respect to Claim 40, the additional elements include that "the mappings are modified at the hardware interface independently of the operation system". To the extent that Lebeck teaches that the mappings may be modified, Lebeck discloses that the mappings are modified by the operation system, section 6.3. Accordingly, Applicants respectfully submit that Claim 40 contains limitations that are not disclosed by Lebeck and therefore is patentable over Lebeck.

With respect to Claim 41, the additional limitations include "refreshing the content of physical memory devices by the hardware interface independently of the operating system." Those skilled in the art appreciate that, because the mappings are created and modified by a hardware interface between the processor and the memory, the memory may be refreshed independently of the operating system. However, Lebeck discloses that the mappings are created and modified by the operating system. Therefore, the systems and methods of Lebeck do not permit refreshing the content of the memory device independently of the operating system. Accordingly, Applicants respectfully submit that Claim 41 contains limitations that are not disclosed by Lebeck and therefore is patentable over Lebeck.

With respect to Claim 42, the additional limitations include "identifying one or more of the plurality of memory devices referenced by relatively few mappings" and "setting the identified one or more of the plurality of memory devices to a reduced power state." Lebeck does not teach or suggest identifying one or more of the plurality of memory device referenced by relatively few mappings. Instead, Lebeck discloses identifying frequently accessed pages. The frequency of mappings is different from the frequency with which pages are accessed. Lebeck also does not teach or suggest setting the memory devices, identified as a function of the frequency of mappings thereto, to a reduced power state. Instead, Lebeck discloses that pages are reassigned as a function of page access frequency, section 4. Furthermore, Lebeck discloses that a reduced power state of a given memory device is entered after a threshold period of time has expired from the last access to the given memory device. Accordingly, Applicants

respectfully submit that Claim 42 contains elements that are not disclosed by Lebeck and therefore is patentable over Lebeck.

With respect to Claim 43, the additional limitations include "re-mapping the identified portions of the processor's physical address space to physical memory by the hardware interface in a manner that reduces the number of physical memory devices referenced by the identified portions of the processor's physical address space." Lebeck does not teach that the remapping is done at a hardware interface. Instead, Lebeck discloses that reassignment is performed by the operating system. Accordingly, Applicants respectfully submit that Claim 43 contains elements that are not disclosed by Lebeck and therefore is patentable over Lebeck

With respect to Claim 44, the additional limitations include that "the re-mapping is periodically performed after a pre-defined number of memory references." To the extent that Lebeck may teach re-mapping the logical address space to the physical address space, Lebeck discloses that the re-mapping is performed one time, section 4. With respect to Claim 45, the additional limitations include that "the re-mapping is performed after power consumption by the physical memory reaches a determined threshold." Lebeck does not teach or suggest re-mapping the logical address space to the physical address space after power consumption by the physical memory reaches a determined threshold. With respect to Claim 46, the additional limitations include that "the re-mapping is periodically performed after a pre-defined number of memory allocations." To the extent that Lebeck may teach re-mapping the logical address space to the physical

address space, the re-mapping is unrelated to the allocation status of memory. With respect to Claim 47, the additional limitations include that "the re-mapping is performed at periodic time intervals." To the extent that Lebeck may teach re-mapping the logical address space to the physical address space, Lebeck discloses that the re-mapping is performed one time, section 4. Applicants respectfully submit that Claims 44, 45, 46 and 47 each contain elements that are not disclosed by Lebeck and therefore are patentable over Lebeck.

For the above-advanced reasons, Applicants assert that Claims 2 and 39-47 are patentably distinguishable over Lebeck. Accordingly, Applicants respectfully request that the §102(a) rejection of Claims 2 and 39-47 be withdrawn and Claims 2 and 39-47 be allowed.

Claim 3

Claim 3, as amended, recites "a memory controller" comprising "means for receiving memory instructions from a processor . . .". Claim 3 has been rejected as being anticipated by Lebeck. However, as already discussed above, to the extent that Lebeck performs reassignment, such reassignment is performed *by* the processor itself. Lebeck does not show a memory controller that receives addresses from a processor and that also includes "means for mapping . . ." as also recited by claim 3. Accordingly, Lebeck does not disclose each and every element of claim 3, and the §102 rejection of claim 3 is therefore unfounded. Allowance of claim 3 is therefore requested.

Claims 4-9, 12, 16, 37 and 38

Dependent Claims 4-9, 12, 16, 37 and 38 are allowable by virtue of their dependency on respective base Claim 3, as well as the additional elements they recite. Allowance of these claims is respectfully requested.

Claim 17

Claim 17, as amended, recites "monitoring memory accesses received from a processor to identify portions of the processor's address space based on usage " and "periodically re-mapping the processor's address space to physical memory to reduce the number of physical memory devices referenced by the identified portions of the processor's address space." As already discussed, to the extent that Lebeck performs reassignment of physical memory, such reassignment is done by the processor itself. Lebeck describes no process in which memory instructions are received from a processor and remapped at that point to physical memory. Accordingly, Lebeck does not show each and every element of claim 17, and claim 17 should therefore be allowed.

Claims 18-21, 23, 25 and 37

Dependent Claims 18-21, 23 and 25 are allowable by virtue of their dependency on respective base Claim 17, as well as the additional elements they recite. Accordingly, Applicants respectfully request that the §102(a) rejection of Claims 18-21, 23 and 25 be withdrawn and Claim s18-21, 23 and 25 be allowed.

Claim 26

Claim 26, as amended, recites a "memory controller configured to map allocated portions of the logical address space to corresponding portions of

physical address space in a manner that tends to reduce the number of physical memory devices referenced by the allocated portions of the logical address space" and "the memory controller further configured to move portions of memory regions corresponding to allocated portions of the logical address space in response to identification of de-allocated portion of the logical address space and re-mapping the corresponding portions of the physical address space and corresponding portion of the logical address space to reduce the number of physical memory devices referenced by allocated portion of logical memory." Applicants respectfully assert that Lebeck does not teach or suggest allocating memory in a manner that tends to reduce the number of physical memory device referenced by the allocated portion of the logical address space. Instead, Lebeck discloses storing pages in memory in a manner that tends to reduce the number of physical memory devices. Storing pages in memory and allocating memory are not equivalent. Lebeck also does not teach or suggest moving portion of the logical address space when memory is de-allocated and re-mapping the corresponding portions to reduce the number of physical memory devices referenced. Instead, Lebeck discloses reassigning memory based upon the frequency at which the stored pages are accessed.

For the above-advanced reasons, Lebeck does not teach or suggest a "memory controller configured to map allocated portions of the logical address space to corresponding portions of physical address space in a manner that tends to reduce the number of physical memory devices referenced by the allocated portions of the logical address space" or "the memory controller further configured to move portions of memory regions corresponding to allocated

portions of the logical address space in response to identification of de-allocated portion of the logical address space and re-mapping the corresponding portions of the physical address space and corresponding portion of the logical address space to reduce the number of physical memory devices referenced by allocated portion of logical memory." Therefore Applicants respectfully submit that Claim 26 is patentable over Lebeck. Applicants respectfully request that the §102(a) rejection of Claim 26 be withdrawn and Claim 26 be allowed

Claims 33-36

Dependent Claims 33-36 are allowable by virtue of their dependency on respective base Claim 26, as well as the additional elements they recite. Accordingly, Applicants respectfully request that the §102(a) rejection of Claims 33-36 be withdrawn and Claims 33-36 be allowed.

Claim Rejection under 35 U.S.C. § 103

Claims 8 stands rejected under 35 U.S.C. § 103 as being obvious in view of "Power Aware Page Allocation" by Lebeck et al., "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa and U.S. Patent 6,167,484 to Boyer. Dependent Claim 8 is allowable by virtue of its dependency on respective base Claim 3. Accordingly, Applicants respectfully request that the §103(a) rejection of Claim 8 be withdrawn and Claim 8 be allowed.

Conclusion

Claims 1-9, 12, 16-21, 23, 25, 26 and 29-47 are in condition for allowance, subject to a potential terminal disclaimer. Applicants respectfully request prompt indication of allowance of the subject application. If any issue remains unresolved that would prevent allowance of this case, **the Examiner is requested to contact the undersigned attorney to resolve the issue**.

Respectfully Submitted,

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By: _____

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